Department of Higher Education
University of Computer Studies, Yangon
First Year (B.C.Sc./B.C.Tech.)
Final Examination
Digital Logic Fundamentals I (CST-101)
September, 2018

Answer *all* questions. **Time allowed: 3 hours**

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1 Answer **ALL** questions. (20 marks)

a) A pulse in a certain waveform has a frequency of 50 Hz. It repeats itself every
(i) 1 ms (ii) 20 ms (iii) 50 ms (iv) 100 ms

b) The time interval between the 50% points on the rising and falling edges is
(i) rise time (ii) fall time (iii) pulse width (iv) period

c) In the 2's complement form, the binary number 10010011 is equal to the decimal number
(i) -19 (ii) + 109 (iii) + 91 (iv) -109

d) The binary number 1000110101000110111 can be written in hexadecimal as
(i) $AD467_{16}$ (ii) $8C46F_{16}$ (iii) $8D46F_{16}$ (iv) $AE46F_{16}$

e) Once you measure the period of a pulse waveform, the frequency is found by
(i) using another setting (ii) measuring the duty cycle
(iii) finding the reciprocal of the period (iv) using another type of instrument

f) The Boolean expression A + B + C is
(i) a sum term (ii) a literal term (iii) an inverse term (iv) a product term

g) The domain of the expression $A\overline{B}CD + A\overline{B} + \overline{C}D + B$ is
(i) A and D (ii) B only (iii) A, B, C, and D (iv) none of these

h) The Boolean expression X = (A + B)(C + D) represents
(i) two ORs ANDed together (ii) two ANDs ORed together
(iii) A 4-input AND gate (iv) a 4-input OR gate

i) The output expression for an AND-OR circuit having one AND gate with inputs A, B and C and one AND gate with inputs D, E and F is
(i) $\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$ (ii) $(\overline{A} + \overline{B} + \overline{C})(\overline{D} + \overline{E} + \overline{F})$ (iii) ABC + DEF (iv) (A + B + C)(D + E + F)

j) A full-adder is characterized by
(i) two inputs and two outputs (ii) three inputs and two outputs
(iii) two inputs and three outputs (iv) two inputs and one output

2 (a) A portion of a periodic digital waveform is shown in Figure 2(a). The measurements are in milliseconds. Determine (i) period (ii) frequency (iii) duty cycle (10 marks)

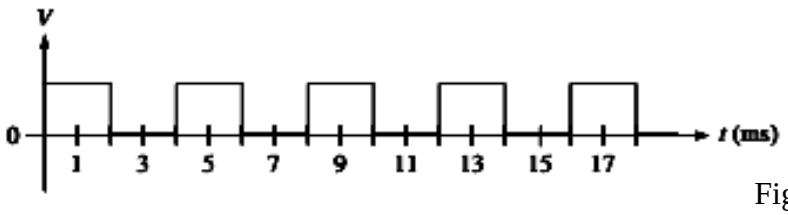


Figure 2(a)

(b) (i) Subtract 173_{16} from BCD_{16}.
(ii) Determine the decimal value of the sign-magnitude number 01110111.
(iii) Add the BCD numbers: 01001000 + 00110100. (10 marks)

3 (a) (i) Describe the functional difference between a NOR gate and a negative-AND gate. Do they both have the same truth table?
(ii) Write the output expression for a 3-input NOR with input variables A, B, and C. (9 marks)

(b) (i) Determine the total number of possible input combinations for a 4-input AND gate.
(ii) The waveforms in Figure 3(b) are applied to points A and B of a 2-input AND gate followed by an inverter. Draw the output waveform.

(6 marks)

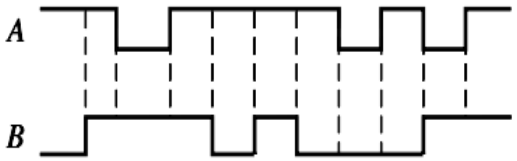


Fig. 3(b)

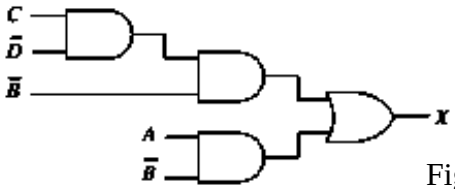


Fig. 4(b)

4 (a) (i) Develop a truth table for standard POS expression: $(A+\overline{B}+C)(A+B+\overline{C})(\overline{A}+\overline{B}+\overline{C})$ (ii) Convert the standard POS expression in (i) to an equivalent SOP expression. (iii) Use Karnaugh map to simplify the standard SOP expression in (ii). (10 marks)

(b) Write the Boolean expression for the logic circuits in Figure 4(b). (5 marks)

5 (a) Implement the expression $X=\overline{(\overline{A}+\overline{B}+\overline{C})DE}$ by using NAND logic.

(9 marks)

(b) Simplify the circuit in Figure 5(b) as much as possible.

(6 marks)

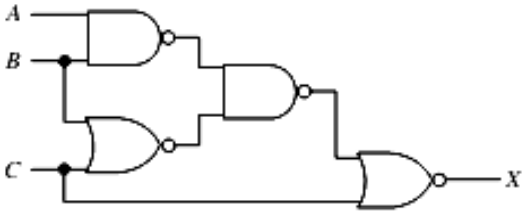


Fig. 5(b)

6 (a) (i) A 3-line-to-8-line decoder can be used for octal-to-decimal decoding. When a binary 101 is on the inputs, which output line is activated? (ii) Show the decoding logic for 000101 codes if an active-HIGH (1) output is required. (6 marks)

(b) BCD numbers are applied sequentially to the BCD-to-decimal decoder in Figure 6(b). Draw a timing diagram, showing each output in the proper relationship with the others and with the inputs.

(9 marks)

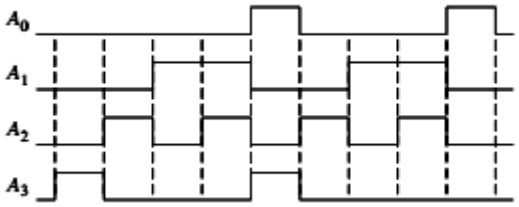
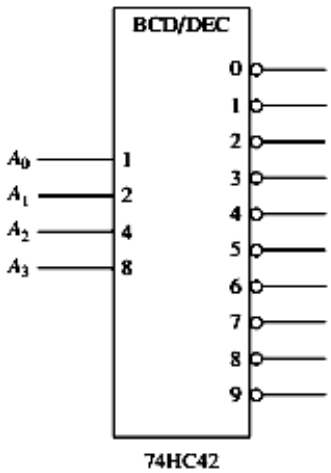


Fig. 6(b)



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